REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 14-02-18	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, RS-232 TRANSCEIVER WITH SPLIT SUPPLY PIN FOR LOGIC SIDE, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/13621**
	REV	**PAGE** 1 **OF** 15

AMSC N/A

5962-V045-14

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance RS-232 transceiver with split supply pin for logic side microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13621	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	TRS3253E-EP	RS-232 transceiver with split supply pin for logic side

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	Package style
X	32	Plastic quad flatpack no-lead

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{CC} to GND	-0.3 V to 6.0 V
VL to GND	-0.3 V to V_{CC} + 0.3 V
V+ to GND	-0.3 V to 7.0 V
V- to GND	0.3 V to -7.0 V
Maximum V+ + |V-|	13.0 V 2/
Input voltage, (V_I):	
DIN, $\overline{\text{FORCEOFF}}$ to GND, FORCEON to GND	-0.3 V to 6.0 V
Maximum RIN to GND	±25.0 V
Output voltage, (V_O):	
Maximum DOUT to GND	±13.2 V
ROUT	-0.3 V to V_L + 0.3 V
Junction temperature, (T_J)	150°C
Storage temperature, (Tstg)	-65°C to 150°C
Typical ESD protection, (RIN, DOUT):	
Human Body Model	±15 kV
IEC 61000-4-2 Air Gap discharge	±8 kV
IEC 61000-4-2 Contact discharge	±8 kV

1.4 Recommended operating conditions.

Supply voltage, (V_{CC})	3.0 V to 5.5 V
Supply voltage, (V_L)	1.65 V to V_{CC}
Maximum input logic threshold low, (DIN, $\overline{\text{FORCEOFF}}$, FORCEON):	
V_L = 3.0 V or 5.5 V	0.8 V
V_L = 2.3 V	0.6 V
V_L = 1.65 V	0.5 V
Minimum input logic threshold high, (DIN, $\overline{\text{FORCEOFF}}$, FORCEON):	
V_L = 5.5 V	2.4 V
V_L = 3.0 V	2.0 V
V_L = 2.3 V	1.4 V
V_L = 1.65 V	1.25 V
Operating temperature	-55°C to 125°C
Receiver input voltage	-25 V to 25 V

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ V+ and V- can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

2. APPLICABLE DOCUMENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION (IEC)

IEC 61000-4-2 – Testing and measurement techniques –Electrostatic discharge immunity test

(Copies of these documents are available online at http:/www.iec.ch or IEC Regional Center for America (IEC-ReCNA) , 446 Main St., 16th Floor, Worcester, MA 01608).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Function table. The function table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 Driver slew rate. The driver slew rate shall be as shown in figure 6.

3.5.7 Driver pulse skew. The driver pulse skew shall be as shown in figure 7.

3.5.8 Receiver propagation delay times. The receiver propagation delay times shall be as shown in figure 8.

3.5.9 Receiver enable and disable times. The receiver enable and disable times shall be as shown in figure 9.

3.5.10 $\overline{\text{INVALID}}$ propagation delay times and supply enabling time. The $\overline{\text{INVALID}}$ propagation delay times and supply enabling time shall be as shown in figure 10.

TABLE I. Electrical performance characteristics. 1/

Test		Symbol	Test conditions 2/		Limits			Unit
					Min	Typ 3/	Max	
Electrical characteristics 4/								
Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON	I_I				±0.01	±2.9	µA
Supply current (T_A = 25°C)	Auto powerdown plus disabled	I_{CC}	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}			0.5	1.11	mA
	Power off					1	10	µA
	Auto powerdown plus enabled					1	10	
RECEIVER SECTION 5/ 6/								
Electrical characteristics								
Output leakage current		I_{off}				±0.05	±25	µA
Output voltage low		V_{OL}					0.4	V
Output voltage high		V_{OH}			V_L – 0.6	V_L – 0.1		V
Input threshold low		V_{IT-}	T_A = 25°C	V_L = 5 V	0.8	1.2		V
				V_L = 3.3 V	0.6	1.5		V
Input threshold high		V_{IT+}	T_A = 25°C	V_L = 5 V		1.8	2.4	V
				V_L = 3.3 V		1.5	2.4	V
Input hysteresis		V_{hys}				0.5		V
Input resistance			T_A = 25°C		3	5	7	kΩ
Switching characteristics								
Receiver propagation delay		t_{PHL}	Receiver input to receiver output			0.15		µs
		t_{PLH}	C_L = 150 pF			0.15		
Receiver skew		t_{PHL} - t_{PLH}				50		ns
Receiver output enable time		t_{en}	From $\overline{\text{FORCEOFF}}$			200		ns
Receiver output disable time		t_{dis}	From $\overline{\text{FORCEOFF}}$			200		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 5/		Limits			Unit
				Min	Typ	Max	
DRIVER SECTION							
Electrical characteristics							
Output voltage swing	V_{OH}	All driver output load with 3 kΩ to ground, V_{CC} = 3.1 V to 5.5 V		±5	±5.4		V
Output resistance	r_O	V_{CC} = V+ = V- = 0, Driver output = ±2V		300	10M		Ω
Output short circuit current	I_{OS}	V_{T_OUT} = 0				±60	mA
Output leakage current	I_{OZ}	V_{T_OUT} = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 3 V to 3.6 V				±25	µA
		V_{T_OUT} = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 4.5 V to 5.5 V					
Driver input hysteresis						0.5	V
Input leakage current		DIN, $\overline{\text{FORCEOFF}}$, FORCEON			±0.01	±2.9	µA
Timing requirements							
Maximum data rate		R_L = 3 kΩ, C_L = 200 pF, One driver switching		1000			kbps
Time to exit powerdown		$\|V_{T\_OUT}\|$ > 3.7 V			100		µs
Driver skew 7/	$\|t_{PHL} - t_{PLH}\|$				100		ns
Transition region slew rate		V_{CC} = 3.3 V, T_A = 25°C, RL = 3 kΩ to 7 kΩ, Measured from 3 V to -3V or -3 V to 3 V	C_L = 150 pF to 1000 pF	15		150	V/µs
AUTO POWERDOWN SECTION							
Electrical characteristics 6/ 8/ (See FIGURE xx)							
Receiver input threshold for $\overline{\text{INVALID}}$ high level output voltage	$V_{T+(valid)}$	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L				2.7	V
Receiver input threshold for $\overline{\text{INVALID}}$ high level output voltage	$V_{IT-(valid)}$	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L		-2.7			
Receiver input threshold for $\overline{\text{INVALID}}$ low level output voltage	$V_{T(invalid)}$	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L		-0.3		0.3	
$\overline{\text{INVALID}}$ high level output voltage	V_{OH}	I_{OH} = -1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L		V_L – 0.6			
$\overline{\text{INVALID}}$ low level output voltage	V_{OL}	I_{OH} = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L				0.4	
Switching characteristic 6/ 8/ (See FIGURE xx)							
Propagation delay time, low to high level output	t_{valid}				0.1		µs
Propagation delay time, high to low level output	$t_{invalid}$				50		
Supply enable time	t_{en}				25		
Receiver or driver edge to auto powerdown plus	t_{dis}				30		µs

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Over operating free air temperature range, $V_{CC} = V_L = 3$ V to 5.5 V, C1 – C4 = 0.1 µF (tested at 3.3 V ±10%), C1 = 0.047 µF, C2 – C4 = 0.33 µF (tested at 5 V ±10%) (unless otherwise noted).

3/ All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25°C$.

4/ Testing supply conditions are C1-C4 = 0.1 µF at $V_{CC} = 3.3$ V ±0.15 V; C1-C4 = 0.22 µF at $V_{CC} = 3.3$ V ±0.3 V, and C1 = 0.047 µF and C2-C4 = 0.33 µF at $V_{CC} = 5$ V ±0.5 V.

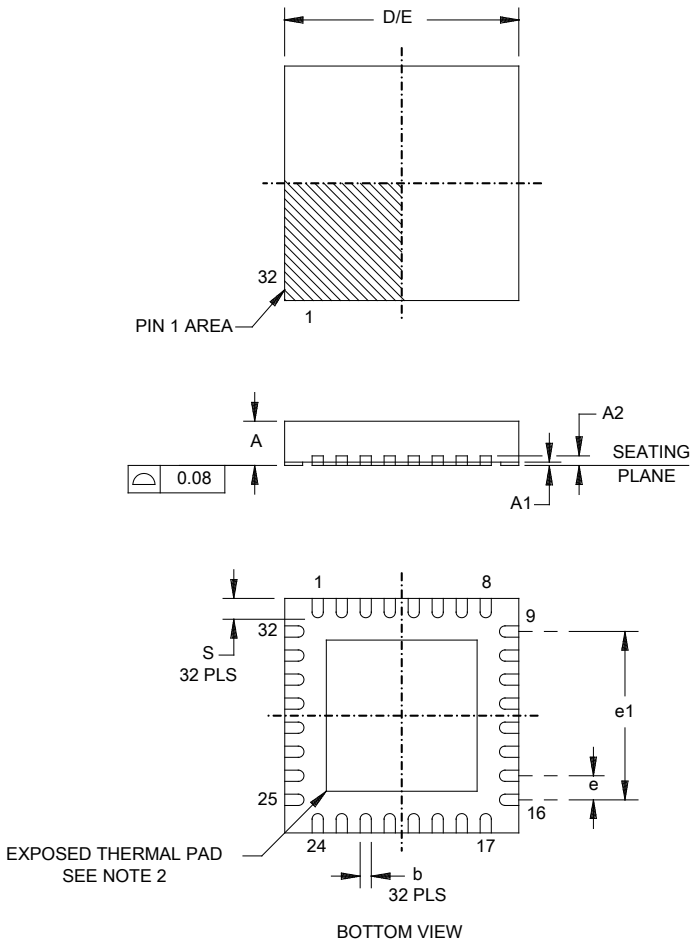
5/ Over operating free air temperature range, $V_{CC} = V_L = 3$ V to 5.5 V, C1 – C4 = 0.1 µF (tested at 3.3 V ±10%), C1 = 0.047 µF, C2 – C4 = 0.33 µF (tested at 5 V ±10%), $T_A = T_{MIN}$ to T_{MAX} (unless otherwise noted).

6/ Typical values are at $V_{CC} = V_L = 3.3$ V, $T_A = 25°C$

7/ Driver skew is measured at the driver zero cross point.

8/ Over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted).

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A	0.80	1.00	D/E	3.85	4.15
A1	0.00	0.05	e	0.40 BSC	
A2	0.20 NOM		e1	2.80 BSC	
b	0.15	0.25	S	0.30	0.50

NOTES:
1. All linear dimensions are in millimeters.
2. The package thermal pad must be soldered to the board for thermal and mechanical performance. See manufacturer data sheet for details regarding the exposed thermal pad dimensions.
3. This drawing is subject to change without notice..

FIGURE 1. Case outline.

Case outline X							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	C2+	9	FORCEON	17	RIN5	25	DOUT1
2	C2-	10	ROUT5	18	RIN4	26	GND
3	V-	11	ROUT4	19	RIN3	27	V_{CC}
4	DIN1	12	ROUT3	20	RIN2	28	$\overline{\text{FORCEOFF}}$
5	DIN2	13	ROUT2	21	RIN1	29	C1+
6	$\overline{\text{INVALID}}$	14	ROUT1	22	DOUT3	30	V+
7	DIN3	15	VL	23	DOUT2	31	C1-
8	NC	16	NC	24	NC	32	NC

FIGURE 2. Terminal connections.

Terminal		Description
Name	RSM	
C1+, C2+	29, 1	Positive terminal of the voltage-doubler charge pump capacitor
V+	30	5.5 V supply generated by the charge pump
C1-, C2-	31, 2	Negative terminal of the voltage doubler charge pump capacitor
INVALID	6	Invalid output pin
V-	3	-5.5 V supply generated by the charge pump
DIN1, DIN2, DIN3,	4 5 7	Driver inputs
ROUT5 – ROUT1	10, 11, 12, 13, 14	Receiver outputs. Swing between 0 and V_L
VL	15	Logic level supply. All CMOS inputs and outputs are reference to this supply.
RIN5 – RIN1	1517, 18, 19, 20, 21	RS-232 receiver inputs
DOUT3, DOUT2, DOUT1	22 23 25	RS-232 driver outputs
GND	26	Ground
VCC	27	3 V to 5.5 V supply voltage
$\overline{\text{FORCEOFF}}$	28	Powerdown Control input (Refer to truth table)
FORCEON	9	Powerdown Control input (Refer to truth table)

FIGURE 3. Terminal functions.

Each Driver

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	Time elapsed since last RIN or DIN transition		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with
H	H	H	X	L	auto powerdown plus disabled
L	L	H	<30 µs	H	Normal operation with
H	L	H	<30 µs	L	auto powerdown plus enabled
L	L	H	>30 µs	Z	Power off by
H	L	H	>30 µs	Z	auto-powerdown plus feature

H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver

INPUTS			OUTPUTS	RECEIVER STATUS
RIN1-RIN5	$\overline{\text{FORCEOFF}}$	Time elapsed since last RIN or DIN transition	ROUT1 – ROUT5	
X	L		Z	Powered off
L	H	<30 µs	H	Normal operation with
H	H	<30 µs	L	auto powerdown plus
Open	H	<30 µs	H	disabled/enabled

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

FIGURE 4. Function tables.

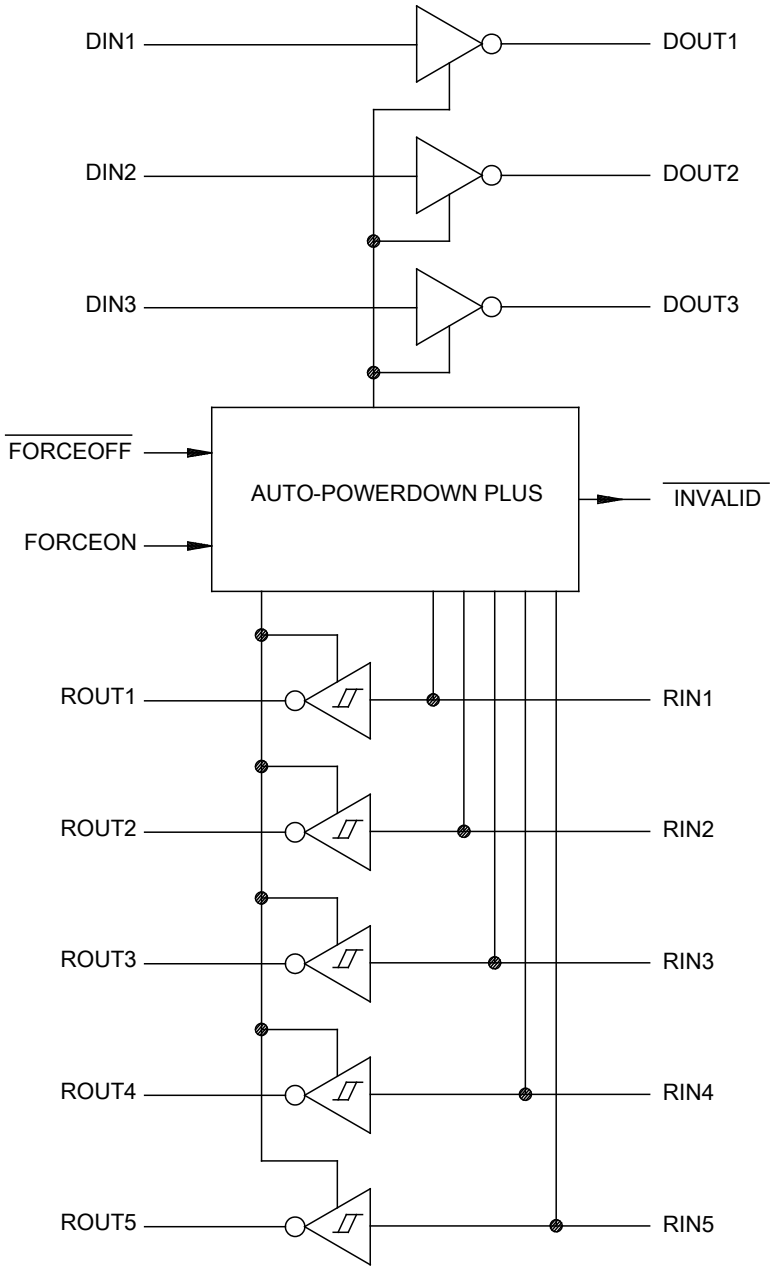
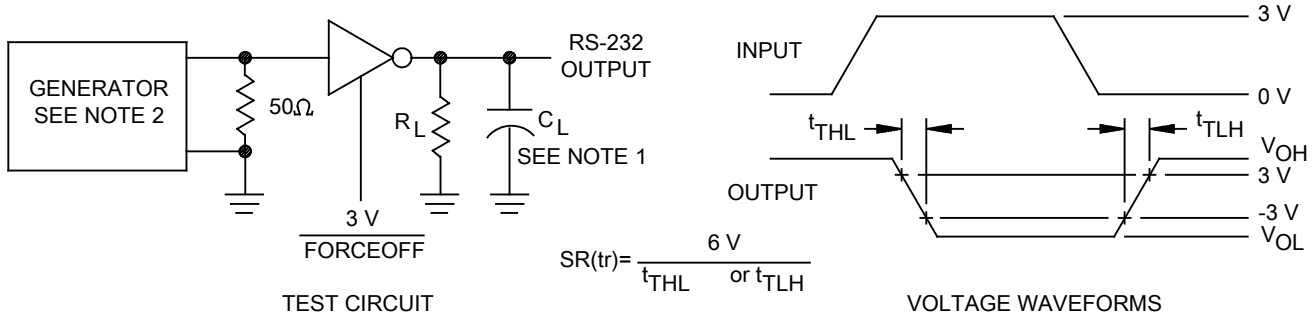
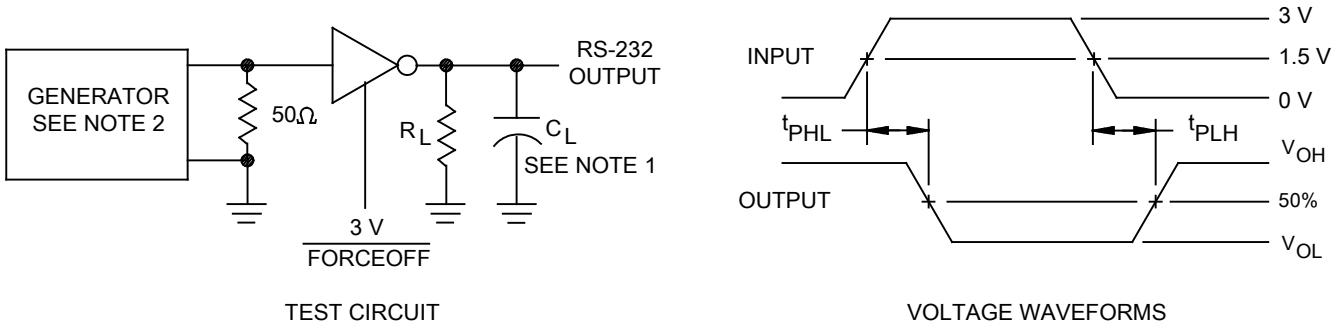


FIGURE 5. Functional block diagram.



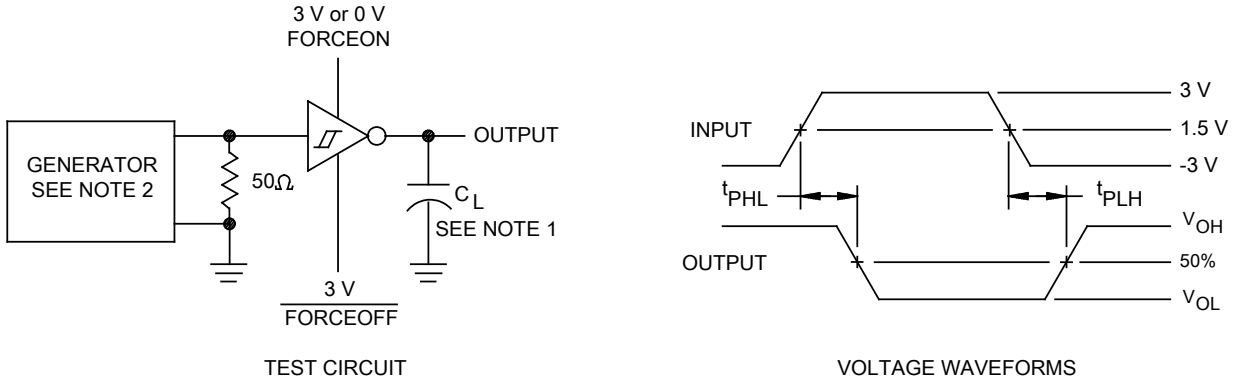
NOTES:
1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

FIGURE 6. Driver slew rate.



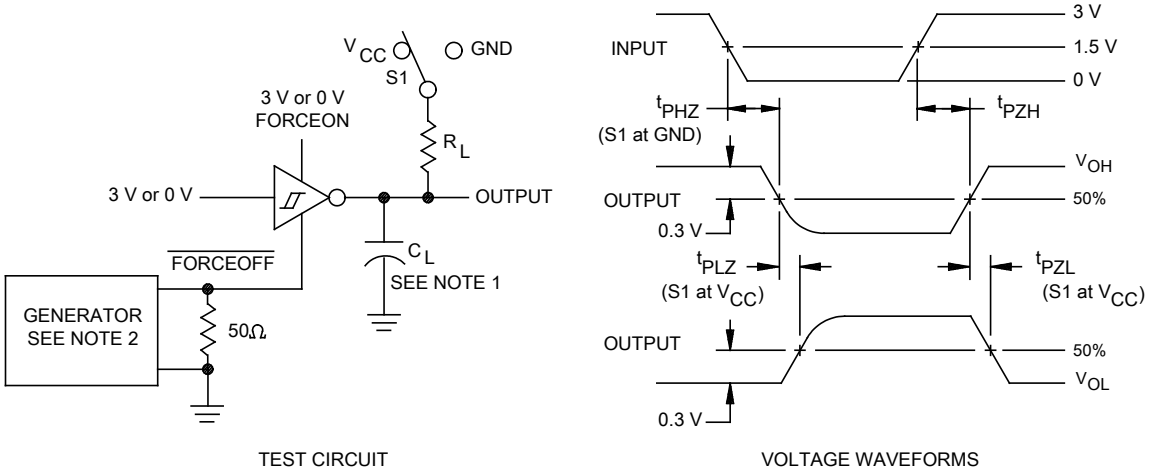
NOTES:
1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

FIGURE 7. Driver pulse skew



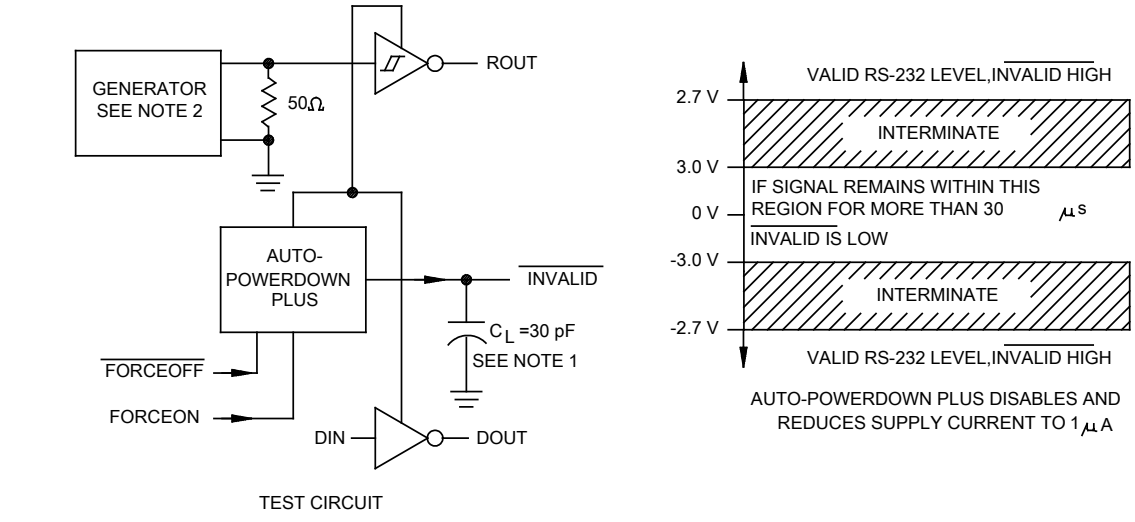
NOTES:
1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
3. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
4. t_{PZL} and t_{PZH} are the same as ten.

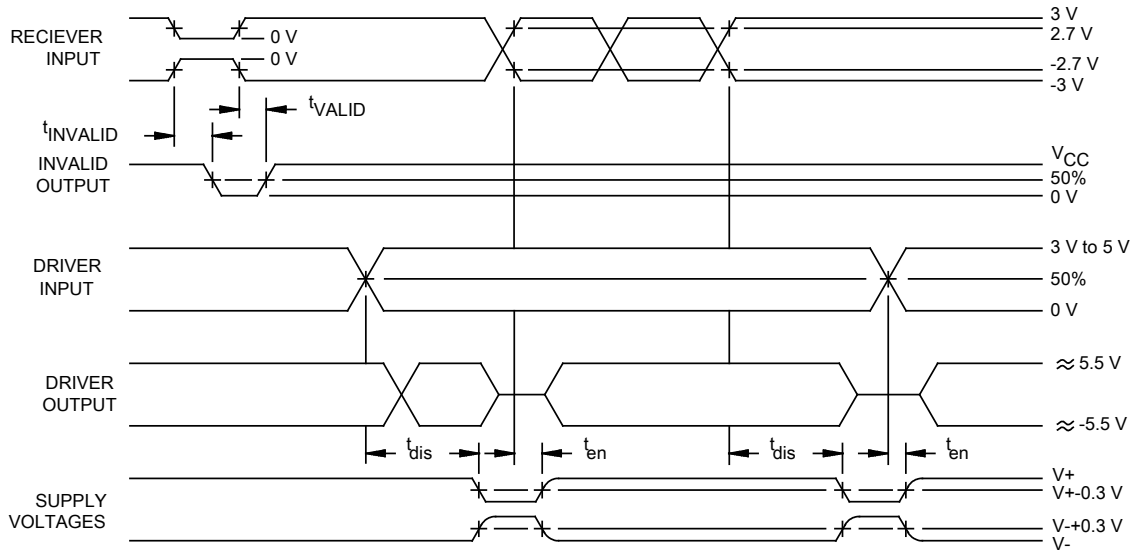
FIGURE 8. Receiver propagation delay times



NOTES:
1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

FIGURE 9. Receiver enable and disable times





NOTES:
1. C_L includes probe and jig capacitance.
2. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

FIGURE 10. $\overline{\text{INVALID}}$ propagation delay times and supply enabling time.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number	Top Side Marking
V62/13621-01XE	24355	TRS3253EMRSMREP	RS53EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493